



Cellot Inc

Cellot

FPCL

Field Programmable Cell Logic

From Idea to Product & ASIC

The FPCL ASIC

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The FPCL and the ASIC

The migration from FPCL to ASIC entry is automatic, quick, and will not require a new technology that frequently creates new “vicious circles” of re-design and debugging. Nevertheless, our solution meets the trend in the market of extended usage in Programmable Devices as a replacement to ASIC. Our low cost and high performance chips, will give us the advantage in competing on certain ASIC market share.

An ASIC – FPCL combination that will enable Application Specific with programmable capabilities can be customized to clients’ needs. As seen in the FFT example, applications can be implemented using core only, which provide advantages over technologies that must have accessories to implement complex applications.

Migration to ASIC

The incentive to migrate from FPCL to ASIC (Application Specific Integrated Circuit) is reduced the larger the applicability of the FPCL device is. However, if this conversion is needed, a straight forward procedure results with an RTL file ready for ASIC. The direct ASIC related advantage of creating an ASIC using the FPCL first as a prototype lays in the fact that the ASIC is manufactured with the same timing related components as the prototype, so a lot of ASIC development time is saved. As the simulation is one to one and fast and the tools are powerful (Please refer to the FPCL Developer Environment documentation), one may want to design his application on Cellot Development Environment without implementing an actual special hardware environment before an ASIC is ready.

Structured Cellot ASIC

The FPCL can be easily converted into ASIC. Nevertheless, a ROM-based device can be prepared to be similar to a Field Programmable device (an FPCL). Once the application is satisfied and tested in its environment, only very limited amount of masks are required to set the ROMs to the specified values and eliminate most of the matrix, remaining with only the needed number of connections. Such methodology will provide a very powerful non-expensive device.

Future Geometry

The FPCL technology offers an “Ever Green” solution. Unlike most of the existing Electronic Designs, our hardware architecture, the core-IPs and the user developed applications are chip geometry independent. Along with future industry technological evolution, and with the introduction of new geometries, a new design will not be required. An FPCL complex design of today may be “as is” ported and implemented on future FPCL devices, years from now. This feature will provide customers with incredible savings and incentive to use the FPCL devices. This feature results from the fractal like architecture: when smaller cells are created in one geometry, these smaller cells can be combined to create larger cells. On the other hand – larger cells can always seamlessly function as smaller cells.